```
  (FILE 'USPAT' ENTERED AT 15:10:29 ON 23 MAR 1999)
                ACT SN990414/L
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L1   (      1935)SEA FILE=USPAT SCHEDUL? (P) ?INSTRUCTION?
L2   (       229)SEA FILE=USPAT 395/800.23/CCLS
L3   (        69)SEA FILE=USPAT L1 AND L2
L4   (       580)SEA FILE=USPAT SUPERSCALAR OR SUPER SCALAR
L5   (       149)SEA FILE=USPAT L1 AND L4
L6   (       104)SEA FILE=USPAT L5 NOT L3
L7   (       173)SEA FILE=USPAT L3 OR L6
L8   (      3852)SEA FILE=USPAT (TAG#### OR ID)(P) ?INSTRUCTION?
L9   (       102)SEA FILE=USPAT L8 AND L7
L10  (       173)SEA FILE=USPAT L3 OR L6
L11  (       102)SEA FILE=USPAT L8 AND L10
                ---------
L12           48 S L3
L13          270 S L5
L14          104 S (712/23/CCLS OR L2) AND L1
L15          298 S L14 OR L6
L16            0 S L8 AND L15D HID
L17          168 S L8 AND L15
=> d 1-56
```

1. 5,887,166, Mar. 23, 1999, Method and system for constructing a program including a navigation instruction; Soummya Mallick, et al., 709/102 [IMAGE AVAILABLE]

2. 5,887,152, Mar. 23, 1999, Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions; Thang M. Tran, 711/136 [IMAGE AVAILABLE]

3. 5,884,062, Mar. 16, 1999, Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions; Shannon A. Wichman, et al., 712/218 [IMAGE AVAILABLE]

4. 5,884,061, Mar. 16, 1999, Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle; James Henry Hesson, et al., 712/217 [IMAGE AVAILABLE]

5. 5,884,060, Mar. 16, 1999, Processor which performs dynamic **instruction** **scheduling** at time of execution within a single clock cycle; Anantakotiraju Vegesna, et al., 712/215 [IMAGE AVAILABLE]

6. 5,884,059, Mar. 16, 1999, Unified multi-function operation scheduler for out-of-order execution in a **superscalar** processor; John G. Favor, et al., 712/215 [IMAGE AVAILABLE]

7. 5,883,841, Mar. 16, 1999, Selective bit line recovery in a memory array; Dennis L. Wendell, 365/190, 203 [IMAGE AVAILABLE]

8. 5,883,826, Mar. 16, 1999, Memory block select using multiple word lines to address a single memory cell row; Dennis Lee Wendell, et al., 365/63, 51, 230.03 [IMAGE AVAILABLE]

9. 5,881,308, Mar. 9, 1999, Computer organization for multiple and out-of-order execution of condition code testing and setting instructions

out-of-order; Harry Dwyer, III, **712/23** [IMAGE AVAILABLE]

10. 5,881,280, Mar. 9, 1999, Method and system for selecting instructions for re-execution for in-line exception recovery in a speculative execution processor; Rajiv Gupta, et al., 712/244 [IMAGE AVAILABLE]

11. 5,881,261, Mar. 9, 1999, Processing system that rapidly indentifies first or second operations of selected types for execution; John G. Favor, et al., 712/214 [IMAGE AVAILABLE]

12. 5,881,258, Mar. 9, 1999, Hardware compatibility circuit for a new processor architecture; Siamak Arya, 712/209 [IMAGE AVAILABLE]

13. 5,878,266, Mar. 2, 1999, Reservation station for a floating point processing unit; Michael D. Goddard, et al., **712/23** [IMAGE AVAILABLE]

14. 5,878,255, Mar. 2, 1999, Update unit for providing a delayed update to a branch prediction array; Thang M. Tran, et al., 712/240 [IMAGE AVAILABLE]

15. 5,875,326, Feb. 23, 1999, Data processing system and method for completing out-of-order instructions; Hoichi Cheong, et al., 395/591 [IMAGE AVAILABLE]

16. 5,872,985, Feb. 16, 1999, Switching multi-context processor and method overcoming pipeline vacancies; Yasunori Kimura, 395/800.01, 376, 384, 385, 386, 389, 584, 585, 586, 800.24, 800.25, 800.26, 800.27 [IMAGE AVAILABLE]

17. 5,864,697, Jan. 26, 1999, Microprocessor using combined actual and speculative branch history prediction; Jonathan H. Shiell, 395/587 [IMAGE AVAILABLE]

18. 5,864,341, Jan. 26, 1999, Instruction dispatch unit and method for dynamically classifying and issuing instructions to execution units with non-uniform forwarding; Troy Neal Hicks, et al., 395/390 [IMAGE AVAILABLE]

19. 5,860,154, Jan. 12, 1999, Method and apparatus for calculating effective memory addresses; Jeffrey M. Abramson, et al., 711/220; 395/393 [IMAGE AVAILABLE]

20. 5,854,934, Dec. 29, 1998, Optimizing compiler having data cache prefetch spreading; Wei Hsu, et al., 395/709, 705; 711/118, 137, 171, 213, 217; 712/207, 237, 241 [IMAGE AVAILABLE]

21. 5,850,543, Dec. 15, 1998, Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return; Jonathan H. Shiell, et al., 395/585; 712/235 [IMAGE AVAILABLE]

22. 5,848,433, Dec. 8, 1998, Way prediction unit and a method for operating the same; Thang M. Tran, et al., 711/137, 118, 125, 140, 144, 145; 712/1, 200 [IMAGE AVAILABLE]

23. 5,848,269, Dec. 8, 1998, Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data; Tetsuya Hara,

395/586; 711/213, 214; 712/237, 240 [IMAGE AVAILABLE]

24. 5,842,036, Nov. 24, 1998, Circuit and method for **scheduling** **instructions** by predicting future availability of resources required for execution; Glenn J. Hinton, et al., **395/800.23**; 712/216, 217, 218 [IMAGE AVAILABLE]

25. 5,842,022, Nov. 24, 1998, Loop optimization compile processing method; Tadashi Nakahira, et al., 395/709, 705 [IMAGE AVAILABLE]

26. 5,841,712, Nov. 24, 1998, Dual comparator circuit and method for selecting between normal and redundant decode logic in a semiconductor memory device; Dennis L. Wendell, et al., 365/200, 185.09, 189.07 [IMAGE AVAILABLE]

27. 5,838,940, Nov. 17, 1998, Method and apparatus for rotating active instructions in a parallel data processor; Sunil Savkar, et al., 395/392; 712/200, 205, 214, 235 [IMAGE AVAILABLE]

28. 5,835,745, Nov. 10, 1998, Hardware **instruction** **scheduler** for short execution unit latencies; David J. Sager, et al., 395/391; **712/23**, 214, 216, 217 [IMAGE AVAILABLE]

29. 5,832,297, Nov. 3, 1998, **Superscalar** microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations; H. S. Ramagopal, et al., 710/5, 6, 56; **712/23**, 217 [IMAGE AVAILABLE]

30. 5,832,293, Nov. 3, 1998, Processor architecture providing speculative, out of order execution of instructions and trap handling; Valeri Popescu, et al., **395/800.23**; 712/218, 244 [IMAGE AVAILABLE]

31. 5,832,292, Nov. 3, 1998, High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution; Le Trong Nguyen, et al., **395/800.23**; 712/218 [IMAGE AVAILABLE]

32. 5,832,249, Nov. 3, 1998, High performance **superscalar** alignment unit; Thang Tran, et al., 395/380; 712/215 [IMAGE AVAILABLE]

33. 5,831,871, Nov. 3, 1998, Integrated structure layout and layout of interconnections for an instruction execution unit of an integrated circuit chip; Kevin R. Iadonato, et al., 364/491; 327/565; 364/490; 710/29; 712/25, 26, 27, 201, 216 [IMAGE AVAILABLE]

34. 5,828,886, Oct. 27, 1998, Compiling apparatus and method for promoting an optimization effect of a program; Masakazu Hayashi, 395/709, 707 [IMAGE AVAILABLE]

35. 5,828,874, Oct. 27, 1998, Past-history filtered branch prediction; Simon C. Steely, Jr., et al., 395/587 [IMAGE AVAILABLE]

36. 5,826,073, Oct. 20, 1998, Self-modifying code handling system; Amos Ben-Meir, et al., 395/567 [IMAGE AVAILABLE]

37. 5,826,070, Oct. 20, 1998, Apparatus and method for maintaining status flags and condition codes using a renaming technique in an out of order floating point execution unit; Christopher Hans Olson, et al.,

395/563; **712/23**, 217 [IMAGE AVAILABLE]

38. 5,826,055, Oct. 20, 1998, System and method for retiring instructions in a **superscalar** microprocessor; Johannes Wang, et al., 395/394; **712/23** [IMAGE AVAILABLE]

39. 5,822,579, Oct. 13, 1998, Microprocessor with dynamically controllable microcontroller condition selection; Shannon A. Wichman, 395/595 [IMAGE AVAILABLE]

40. 5,822,574, Oct. 13, 1998, Functional unit with a pointer for mispredicted resolution, and a **superscalar** microprocessor employing the same; Thang M. Tran, 395/580; **712/23**, 215, 217, 235, 237, 239 [IMAGE AVAILABLE]

41. 5,819,308, Oct. 6, 1998, Method for buffering and issuing instructions for use in high-performance **superscalar** microprocessors; Chien-Kuo Tien, et al., 711/108, 145; **712/23**, 215 [IMAGE AVAILABLE]

42. 5,819,060, Oct. 6, 1998, Instruction swapping in dual pipeline microprocessor; Joseph Cesana, 395/395 [IMAGE AVAILABLE]

43. 5,819,059, Oct. 6, 1998, Predecode unit adapted for variable byte-length instruction set processors and method of operating the same; Thang M. Tran, 395/389; **712/23**, 210, 217 [IMAGE AVAILABLE]

44. 5,819,057, Oct. 6, 1998, **Superscalar** microprocessor including an instruction alignment unit with limited dispatch to decode units; David B. Witt, et al., 395/380; 712/210, 212, 213, 215 [IMAGE AVAILABLE]

45. 5,819,056, Oct. 6, 1998, Instruction buffer organization method and system; John G. Favor, 395/380; **712/23**, 210, 212, 213 [IMAGE AVAILABLE]

46. 5,812,839, Sep. 22, 1998, Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit; Bradley D. Hoyt, et al., 395/586; 712/235 [IMAGE AVAILABLE]

47. 5,809,450, Sep. 15, 1998, Method for estimating statistics of properties of instructions processed by a processor pipeline; George Z. Chrysos, et al., 702/186; 712/237 [IMAGE AVAILABLE]

48. 5,809,276, Sep. 15, 1998, System and method for register renaming; Trevor A. Deosaran, et al., 395/393; 712/207, 208, 209, 210, 211, 212 [IMAGE AVAILABLE]

49. 5,809,273, Sep. 15, 1998, Instruction predecode and multiple instruction decode; John G. Favor, et al., 395/386; **712/23**, 212, 213 [IMAGE AVAILABLE]

50. 5,805,916, Sep. 8, 1998, Method and apparatus for dynamic allocation of registers for intermediate floating-point results; Soummya Mallick, et al., **395/800.23**; 712/217, 222 [IMAGE AVAILABLE]

51. 5,805,853, Sep. 8, 1998, **Superscalar** microprocessor including flag operand renaming and forwarding apparatus; Scott A. White, et al., 395/394; **712/23**, 215 [IMAGE AVAILABLE]

52. 5,805,849, Sep. 8, 1998, Data processing system and method for using an unique identifier to maintain an age relationship between executing instructions; Paul Joseph Jordan, et al., 395/390; 712/216 [IMAGE AVAILABLE]

53. 5,801,975, Sep. 1, 1998, Computer modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instruction cycles; John S. Thayer, et al., 708/402 [IMAGE AVAILABLE]

54. 5,799,180, Aug. 25, 1998, Microprocessor circuits, systems, and methods passing intermediate instructions between a short forward conditional branch instruction and target instruction through pipeline, then suppressing results if branch taken; Jonathan H. Shiell, et al., 395/581; **712/23**, 218, 219 [IMAGE AVAILABLE]

55. 5,799,165, Aug. 25, 1998, Out-of-order processing that removes an issued operation from an execution pipeline upon determining that the operation would cause a lengthy pipeline delay; John G. Favor, et al., 395/390; **712/23**, 215, 216, 219 [IMAGE AVAILABLE]

56. 5,797,025, Aug. 18, 1998, Processor architecture supporting speculative, out of order execution of instructions including multiple speculative branching; Valeri Popescu, et al., **395/800.23**; 712/205, 212, 215, 216, 217, 234, 239 [IMAGE AVAILABLE]
=>

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L1  (      1935)SEA FILE=USPAT SCHEDUL? (P) ?INSTRUCTION?
L2  (       229)SEA FILE=USPAT 395/800.23/CCLS
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